REMARKS

Claims 49 – 60 are pending. All other claims are canceled and/or withdrawn. Applicant submits the following response to place this case in condition for allowance.

Objections to claim 49 and 52

In claim 49, the Examiner objected to the term "unprocessed wafer"; this objection is traversed, because the Examiner has taken the term out of out context in the claim, and without considering the additional language associated with this term: Claim 49 recites:

> ..... wherein the semiconductor wafer is **an unprocessed wafer having no active circuit layers or interconnect layers present on said top surface or said bottom surface** of the semiconductor wafer... (emphasis added)

Accordingly, the claim clearly sets out that "unprocessed" - in the context of the invention - means a wafer having no active circuit layers or interconnect layers. This is consistent with the terminology used in the specification; thus the presence of a hole in the wafer – without anything else - does not render the wafer "processed" in this instance. The rejection is thus traversed.

With respect to claim 52: the Examiner has slightly misquoted the language of the claim; it actually recites:

> **"...said via is substantially larger than a minimum feature size used in fabricating said active circuit..."**

The term "minimum feature size" is a well-known term of art in the industry, and refers to the minimum resolvable feature on a wafer within the limits of a particular process. These are further defined by each semiconductor manufacturing plant according to a design rule specification. Thus, an active circuit may have a .1 micron minimum poly gate width. One skilled in the art in this field is very knowledgeable and proficient in being able to measure such features on a wafer, regardless of where it is made. The invention of claim 52 merely sets out a relationship between the vias and such minimum sized features, and thus is submitted to be quite clear and definite.

Response to rejections under 102/103

Claims 49 – 50, 52 – 59 were rejected in light of Farnworth – U.S. Patent No. 5,973,396. The characterization of claims 49 – 52 as "product by process" claims is not correct. Applicant is claiming a particular type of wafer which is well suited for later fabrication processes, such as the

fabrication of active devices on such wafer. This is done by including vias, I/O interconnect structures on the wafer which make it easier to avoid certain later packaging operations while there are active devices present.

Thus the claim recites:

> ....wherein the I/O interconnect structure is adapted **such that an active circuit which is fabricated ...at a later time ...** can be electrically connected to another integrated circuit **without requiring further packaging operations** to form pads or bumps ... (emphasis added)

The Examiner is misreading the claim; it does not recite that the wafer includes "..an active circuit." It merely recites that the wafer includes an I/O interconnect structure that is "adapted" so that any later added active circuit can be electrically connected as noted without requiring further packaging operations.

So as an initial matter, Applicants traverse any suggestion or finding that the claims are product by process claims. They are not: they are directed to a wafer which has certain properties and structures adapted for later processing steps; but the later processing steps and the active circuits do not form part of the claim.

With that said the arguments against Farnworth are simply this: the reference does not show the type of wafer set out in claim 49. As the Examiner can verify, reference number 22 in Farnworth refers to an active circuit:

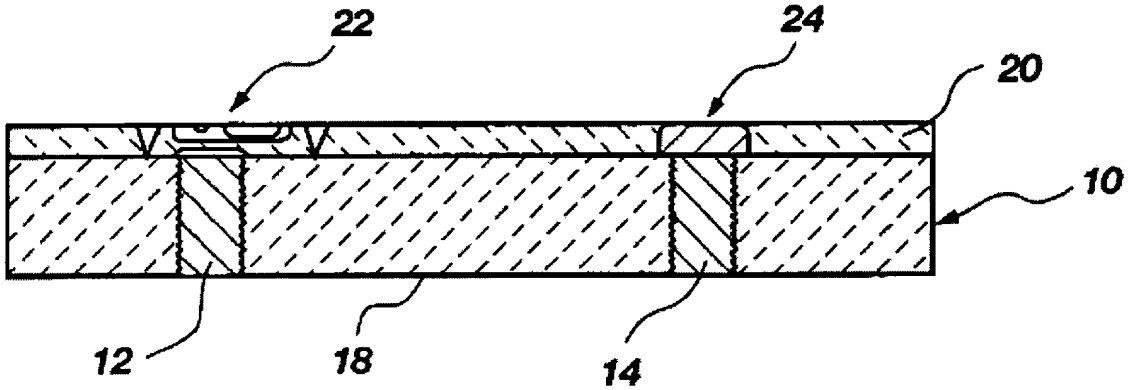
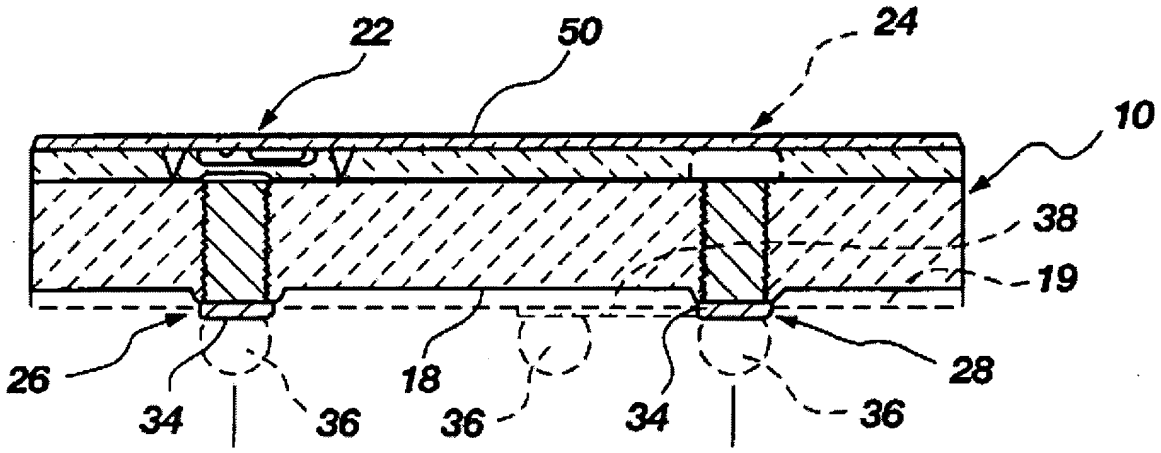


Fig. 1B

See e.g., 5,973,396 at col. 4, ll. 55+. At this point, therefore, Farnworth shows a die (or wafer) which includes active circuits. In the present invention, the wafer does not yet have any active

circuits as can be seen in the claim. So this figure from Farnworth does not show the claimed invention.

Later, Farnworth does add packaging (28, 36) but, again, only after the active circuits 22 are already there:



Accordingly, it should be clear to the Examiner that Farnworth never shows a structure which corresponds to the wafer described in claim 1. Farnworth shows a different structure which already includes active circuits. While embodiments of the present invention could be "processed" to later result in something that looks like Farnworth's embodiment, the converse is not true, and that is why the present invention distinguishes over the reference.

Again as noted in the disclosure, there are several advantages to having a wafer with certain types of packaging already included. This avoids having to add it later, such as after active circuit fabrication.

The Gnadinger reference does not cure this basic deficiency in Farnworth, and the Examiner does not seem to suggest such. For this reason it does not present any meaningful obstacle to patentability.

For this reason Applicant submits that claim 49 adequately distinguishes already over the references of record, so the rejection is traversed.

Claims 50 – 60 depend from claim 49, and should be allowable for at least the same reasons. Moreover, at least as concerns dependent claim 51, the Examiner acknowledges that Gnadinger does not "fill" the vias with insulating material; they are lined along the sidewalls purely for insulation. Thus, they cannot fulfill the "support" function set out in claim 51.

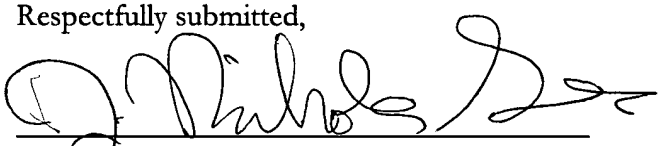
CONCLUSION

The rejections have been fully addressed through the explanation above. Favorable consideration is requested.

A petition and fee for a two month extension of time is also enclosed. Please charge any fees due to deposit account 501-244.

Should the Examiner wish to contact the undersigned at any time to discuss this case, please feel free to use the number identified below.

Respectfully submitted,



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I hereby certify that the foregoing is being deposited with the U.S. Postal Service, postage prepaid, to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, this 26th day of October 2005.